1. A method of forming a dielectric material layer comprising:

depositing a low dielectric constant material layer on a substrate;

implanting silicon ions into said low dielectric constant material layer; and

thereafter depositing a TEOS-based silicon oxide layer overlying said low dielectric constant material whereby there is good adhesion between said low dielectric constant material layer and said TEOS-based silicon oxide layer.

2. The method according to Claim 1 wherein said low dielectric constant material is selected from the group consisting of: porous and non-porous carbon-based silicon oxides, porous and non-porous doped silicon oxides, porous and non-porous organic polymers, and porous and non-porous inorganic polymers.

3. The method according to Claim 1 wherein said low dielectric constant material layer has a thickness of between about 500 and 50,000 Angstroms.

4. The method according to Claim 1 wherein said step of implanting silicon ions into said low dielectric

constant material layer comprises implanting said silicon ions at an energy of between about 5 and 30 KeV at a dosage of between about 1 E 12 and 1 E 16 ions/cm^2.

5. The method according to Claim 1 wherein said silicon ions are implanted into said low dielectric constant material layer to a depth of between about 50 and 600 Angstroms.

6. The method according to Claim 1 wherein said TEOS-based dielectric layer has a thickness of between about 50 and 5000 Angstroms.

7. A method of forming a dielectric material layer comprising:

depositing a low dielectric constant material layer on a substrate; and

depositing a silicon-based dielectric layer overlying said low dielectric constant material wherein said silicon-based dielectric layer is not silicon oxide whereby there is good adhesion between said low dielectric constant material layer and said silicon-based dielectric layer.

8. The method according to Claim 7 wherein said low dielectric constant material is selected from the group consisting of: porous and non-porous carbon-based silicon oxides, porous and non-porous doped silicon oxides, porous and non-porous organic polymers, and porous and non-porous inorganic polymers.

9. The method according to Claim 7 wherein said low dielectric constant material layer has a thickness of between about 500 and 50,000 Angstroms.

10. The method according to Claim 7 wherein said silicon-based dielectric layer is selected from the group consisting of: silicon nitride, silicon carbide, silicon oxynitride, silsesquioxanes, and silicon-rich silicon oxynitride.

11. The method according to Claim 7 wherein said silicon-based dielectric layer has a thickness of between about 50 and 5000 Angstroms.

12. A method of dual damascene copper metallization in the fabrication of an integrated circuit device comprising:

depositing a first low dielectric constant material

layer over a substrate;

implanting silicon ions into said first low dielectric constant material layer;

thereafter depositing a TEOS-based silicon oxide etch stop layer overlying said first low dielectric constant material whereby there is good adhesion between said first low dielectric constant material layer and said TEOS-based silicon oxide etch stop layer;

depositing a second low dielectric constant material layer overlying said etch stop layer;

implanting silicon ions into said second low dielectric constant material layer;

thereafter depositing a TEOS-based silicon oxide capping layer overlying said second low dielectric constant material whereby there is good adhesion between said second low dielectric constant material layer and said TEOS-based silicon oxide capping layer;

forming a dual damascene opening through said capping layer, said second low dielectric constant material layer, said etch stop layer, and said first low dielectric constant material layer; and

forming a barrier metal layer and a copper layer within said dual damascene opening to complete said copper metallization in the fabrication of said integrated circuit device.

13. The method according to Claim 12 wherein said first and second low dielectric constant materials are selected from the group consisting of: porous and non-porous carbon-based silicon oxides, porous and non-porous doped silicon oxides, porous and non-porous organic polymers, and porous and non-porous inorganic polymers.

14. The method according to Claim 12 wherein said first and second low dielectric constant material layers have a thickness of between about 500 and 50,000 Angstroms.

15. The method according to Claim 12 wherein said steps of implanting silicon ions into said first and second low dielectric constant material layers comprises implanting said silicon ions at an energy of between about 5 and 30 KeV at a dosage of between about 1 E 12 and 1 E 16 ions/cm^2.

16. The method according to Claim 12 wherein said silicon ions are implanted into said first and second low dielectric constant material layers to a depth of between about 50 and 600 Angstroms.

17. The method according to Claim 12 wherein said TEOS-based dielectric layer has a thickness of between about 50 and 5000 Angstroms.

18. A method of dual damascene copper metallization in the fabrication of an integrated circuit device comprising:

depositing a first low dielectric constant material layer over a substrate;

depositing a silicon-based dielectric etch stop layer overlying said first low dielectric constant material wherein said silicon-based dielectric etch stop layer is not silicon oxide whereby there is good adhesion between said first low dielectric constant material layer and said silicon-based dielectric etch stop layer;

depositing a second low dielectric constant material layer overlying said etch stop layer;

depositing a silicon-based dielectric capping layer overlying said second low dielectric constant material wherein said silicon-based dielectric capping layer is not silicon oxide whereby there is good adhesion between said second low dielectric constant material layer and said silicon-based dielectric capping layer;

forming a dual damascene opening through said

capping layer, said second low dielectric constant material layer, said etch stop layer, and said first low dielectric constant material layer; and

forming a barrier metal layer and a copper layer within said dual damascene opening to complete said copper metallization in the fabrication of said integrated circuit device.

19. The method according to Claim 18 wherein said first and second low dielectric constant materials are selected from the group consisting of: porous and non-porous carbon-based silicon oxides, porous and non-porous doped silicon oxides, porous and non-porous organic polymers, and porous and non-porous inorganic polymers.

20. The method according to Claim 18 wherein said first and second low dielectric constant material layers have a thickness of between about 500 and 50,000 Angstroms.

21. The method according to Claim 18 wherein said silicon-based dielectric layer is selected from the group consisting of: silicon nitride, silicon carbide, silicon oxynitride, silsesquioxanes, and silicon-rich silicon oxynitride.

22. The method according to Claim 18 wherein said silicon-based dielectric layers have a thickness of between about 50 and 5000 Angstroms.